REMARKS

Re-examination and allowance of the present application is respectfully requested.

Initially, Applicants thank the Examiner for indicating his consideration of the documents in the August 23, 2006 and June 30, 2006 Information Disclosure Statements.

Claims 14-16 and 23-25 stand rejected under 35 U.S.C. §103(a) as being obvious over U.S. Patent 5,654,728 to KANAZAWA. Claims 17-22 stand rejected under 35 U.S.C. §103(a) as being obvious over the combination of KANAZAWA in view of an article by LAI entitled "Resonant Snubber-Based Soft-Switching Inverters for Electric Propulsion Drives". Applicants respectfully traverse both grounds of rejection.

According to a feature of an embodiment of the present invention, as defined in independent claim 14, a driving circuit drives a display panel. The drive circuit includes a frequency reducer that is connected in parallel with a first switching element, that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the first switching element and an inductance component of an interconnector, wherein the charge is supplied to the electrode of the display panel from a recovering capacitor through the first switching element and the interconnector.

According to another embodiment of the invention, defined in claim 15, the driving circuit includes a frequency reducer that is connected in parallel with a second switching element and which is operable to reduce a resonance frequency of an LC resonance that results from a parasitic capacitance of the second switching element and an inductance component of an interconnector, wherein a charge is recovered to a recovering capacitor from an electrode of the display panel through the second switching element and the interconnector.

According to a feature of a still further embodiment of the invention, recited in claim 16, a frequency reducer is connected in parallel with a first switching element that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the first switching element and an inductance component of an interconnector, and another frequency reducer is connected in parallel with a second switching element that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the second switching element and an inductance component of the interconnector. A charge is supplied to an electrode of a display panel from a recovering capacitor through the first switching element and the interconnector. The charge is recovered to the recovering capacitor from the electrode of the display panel through the second switching element and the interconnector.

The embodiment of claim 23 specifies that a frequency reducer is connected in parallel with a first switching element operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the first switching element and an inductance component of an interconnector, in which a charge is supplied to an electrode of a display panel from a recovering capacitor through the first switching element and the interconnector.

The embodiment recited in claim 24 discloses the use of a frequency reducer that is connected in parallel with a second switching element to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the second switching element and an inductance component of an interconnector, in which a charge is recovered to a recovering capacitor from an electrode of a display panel through the second switching element and the interconnector.

The embodiment defined by claim 25 specifies that a frequency reducer is connected in parallel with a first switching element that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the first switching element and an inductance component of an interconnector, and another frequency reducer is connected in parallel with a second switching element that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the second switching element and an inductance component of the interconnector, wherein a charge is supplied to an electrode of a display panel from a recovering capacitor through the first switching element and the interconnector, and the charge is recovered to the recovering capacitor from the electrode of the display panel through the second switching element and the interconnector.

Applicants submit that at least the above-discussed features are neither disclosed or suggested by KANAZAWA et al.

KANAZAWA is directed to a plasma display unit in which switch SW14 comprises a pMOS transistor and switch SW15 comprises an nMOS transistor. Each switch includes a diode for clipping a voltage between a source and a drain of the respective MOS transistor in order to protect the transistor. See, for example, column 6, lines 19-25. As shown in Figs. 2 and 4, diodes D14 and D15 are provided between switches SW14 and SW15 to supply voltage to a Y1-Driver 2521 via switch SW17. See, for example, column 7, lines 31-67.

In setting forth the 35 U.S.C. §103(a) rejection of claims 14-16 and 23-25, the Examiner asserts that the diodes in parallel with switching element SW14 and SW15 of KANAZAWA et al. possess frequency reducing properties as capacitors, and thus, it

would have been obvious to replace a diode with a capacitor to reduce the resonance frequency resulting from parasitic capacitance of a switching element.

Applicants respectfully disagree with the Examiner's assertion. Applicants submit that KANAZAWA et al. is not even concerned with the desirability of reducing a resonance frequency of a switching element, the diodes in KANAZAWA et al. being provided only for the purpose of clipping a voltage between a source and drain of a switching element. Applicants thus submit that the Examiner is attempting to employ impermissible hindsight to assert that it would have been obvious to replace a diode with a capacitor to reduce a resonance frequency of the switching element, as the reference fails to teach or even suggest the desirability of doing what the Examiner suggests.

Applicants further submit that diodes and capacitors have different electrical characteristics, and that diodes do not possess frequency reducing properties as capacitors, as alleged by the Examiner. Thus, Applicants submit that there would have been no motivation at the time of Applicants' invention to replace the diode of KANAZAWA et al. by a capacitor to reduce a resonance frequency of a switching element, as KANAZAWA et al. is not directed to reducing a resonance frequency of a switching element.

In view of the above, Applicants submit that the present invention, as defined by claims 14-16 and 23-25 is not obvious over KANAZAWA et al. Accordingly, the Examiner is respectfully requested to withdraw this ground of rejection, and to indicate the allowability of claims 14-16 and 23-25.

Applicants similarly traverse the 35 U.S.C. §103(a) rejection of claims 17-22, submitting that the article to LAI fails to disclose or suggest that which is lacking in KANAZAWA et al.

According to an embodiment of the instant invention, defined in claim 17, a driving circuit that drives a display panel having an electrode includes a capacitor connected in parallel with a first switching element to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the first switching element and an inductance component of an interconnector, in which a charge is supplied to the electrode of the display panel from a recovering capacitor through the first switching element and the interconnector.

In another embodiment of the invention, defined in claim 18, a capacitor is connected in parallel with a second switching element to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the second switching element and an inductance component of an interconnector, in which a charge is recovered to a recovering capacitor through the second switching element and the interconnector.

In a further embodiment of the invention defined by claim 19, a first capacitor is connected in parallel with a first switching element that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the first switching element and an inductance component of an interconnector, while a second capacitor is connected in parallel with a second switching element that is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the second switching element and an inductance component of the interconnector. A charge is supplied to an electrode of a display panel from a recovering capacitor through the first switching element and the interconnector, with the charge being recovered to the recovering capacitor from the electrode of the display panel through the second switching element and the interconnector.

Claim 20 defines another embodiment of the present invention, in which a capacitor is connected in parallel with a source and a drain of a first transistor operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of the first transistor and an inductance component of an interconnector, in which a charge is supplied to an electrode of a display panel from a recovering capacitor through the first transistor and the interconnector.

Claim 21 defines a variation thereof, in which the capacitor is connected in parallel with a source and a drain of a second transistor, while claim 22 defines another variation, in which a first capacitor is connected in parallel with a source and a drain of a first transistor and a second capacitor is connected in parallel with a source and a drain of a second transistor. Each capacitor is operable to reduce a resonance frequency of an LC resonance resulting from a parasitic capacitance of its respective transistor and an inductance component of the interconnector, wherein a charge is supplied to an electrode of a display panel from a recovering capacitor through the first transistor and the interconnector, and the charge is recovered to the recovering capacitor from the electrode of the display panel through the second transistor and the interconnector.

As discussed above, KANAZAWA et al. fails to disclose reducing a resonance frequency of a switching element. The article to LAI is directed to an electric propulsion drive (such as, for example, an internal combustion engine) and a soft-switching inverter used therewith. Fig. 3 illustrates a single-phase soft-switching inverter in which a resonant capacitor Cr1-Cr4 is provided in parallel to switch S1-S4, respectively. The first paragraph of the left column of page 75 discloses that the resonant capacitor may be externally added or internal stray capacitors, the capacitors allowing the switches to turn

off at a lossless condition. When inductor current exceeds a load current at time t2, switches S2 and S3 are turned off, capacitors Cr2 and Cr3 serve as lossless snubbers to allow a zero-voltage turnoff and to slow down a voltage rise rate (dv/dt).

Applicants submit that LAI is directed to non-analogous art (e.g., electric propulsion systems) and fails to provide any motivation for one skilled in the art of plasma displays to look at the art of inverters for a solution to reduce a resonance frequency of a switching element of a display panel.

Further, as discussed above, KANAZAWA at el. fails to disclose or suggest reducing a resonance frequency of a switching element. Thus, Applicants submit that there is no suggestion of the desirability to adapt the capacitors Cr1-Cr4 of LAI to the circuit of KANAZAWA et al., in the manner suggested by the Examiner, to arrive at the invention defined in claims 17-22. Further, even if one attempted to modify KANAZAWA et al. in the manner suggested by the Examiner, one would not arrive at Applicants' claimed invention, in which a resonance frequency of a switching element is reduced. Accordingly, Applicants respectfully request withdrawal of this ground of rejection.

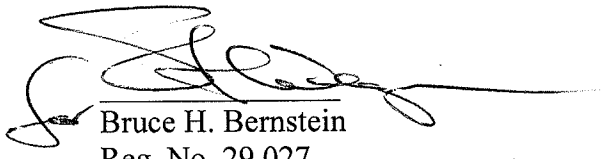
SUMMARY AND CONCLUSION

In view of the fact that none of the art of record, whether considered alone or in combination, discloses or suggests the present invention as now defined by the pending claims, and in further view of the above amendments and remarks, reconsideration of the Examiner's action and allowance of the present application are respectfully requested and are believed to be appropriate.

Should an extension of time be necessary to maintain the pendency of this application, including any extensions of time required to place the application in condition for allowance by an Examiner's Amendment, the Commissioner is hereby authorized to charge any additional fee to Deposit Account No. 19-0089.

If there should be any questions concerning this application, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully Submitted,
Shigeo KIGO et al.



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January 29, 2007
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